VIAVI Solutions

Data Sheet

VIAVI
ATE5800 Series
Testpoint Relay Card (TPR)

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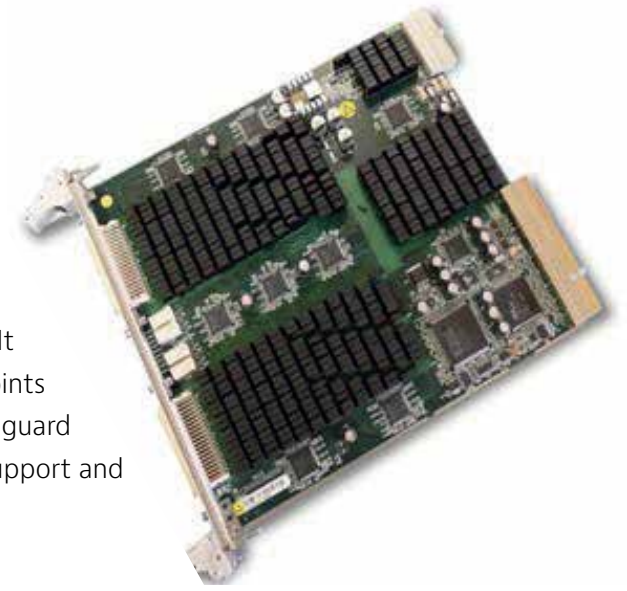
The Testpoint Relay card is the primary analog interface to the Unit Under Test (UUT)

- 192 Test channels
- Non-symmetrical bus structure
- Fast switching time
- Fixture ground connectivity
- Guard amplifier
- General purpose attenuator



The TPR is the primary analog switching interface to the UUT. It routes from 4 global and/or 8 local analog busses to 192 testpoints via a matrix of fast switching relays. The board also contains a guard amplifier, fixture 0V isolation, configuration memory, trigger support and an EEPROM for storage of board specific information.

Module Functionality

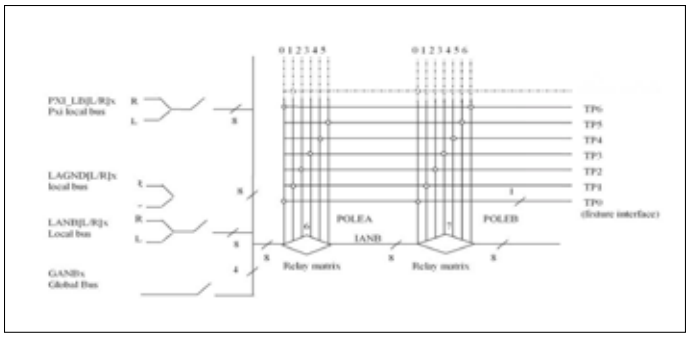
Analog Routing

The four external global analog busses (backplane GANBx), the eight local analog busses (backplane LANB[L/R]x) and the first eight PXI local bus lines (backplane PXI_LB[R/L]x) are reduced to one internal, eight bit wide analog bus (IANB) using relays which also act as the internal/external isolation barrier.

The eight internal analog busses (IANBs) are then connected, via a relay matrix, to two further internal analog busses, one six (POLEA) and the other seven (POLEB) wide. For each bus, each bus component is then connected, via a relay, to a fixture interface output pin.

This means for the six wide bus each bus component connects to 32 output pins whereas the seven wide bus each bus component connects to either 27 or 28 fixture interface outputs (3x28 + 4x27). Each fixture interface output

therefore is attached to two relays, one from each of the internal busses POLEA and POLEB. See the diagram to the right for more details including the analog bus and analog bus ground connections.



Note: By making the (bus) path non-symmetrical it increases the chances of more than two pins (which are guaranteed) being successfully routed from the external analog busses to any particular pin on the fixture interface.

The external global bus connects to the internal analog bus GANBx to IANBx for x=0 to 3 via an isolation relay.

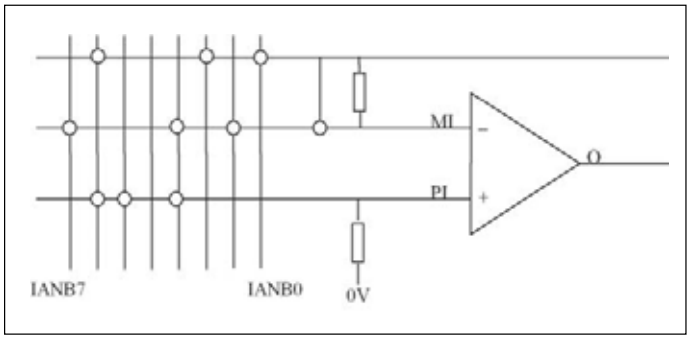
The external local bus connects to the internal analog bus LANB[L/R]x to IANBx for x=0 to 7 via an isolation relay.

The external PXI local bus connects to the internal analog bus PXI_LB[L/R]x to IANBx for x=0 to 7 via an isolation relay.

The relay matrix's are 6x8 (48 relays) and 7x8 (56 relays) creating a full bus interconnect. (The PXI analog bus connections are for selfcheck purposes only).

Guard Amplifier

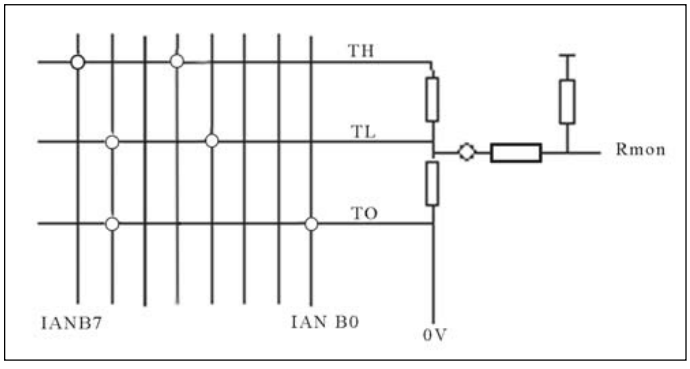
A general purpose guard amplifier is included, connected to the internal common bus (IANB) as follows:



Attenuator

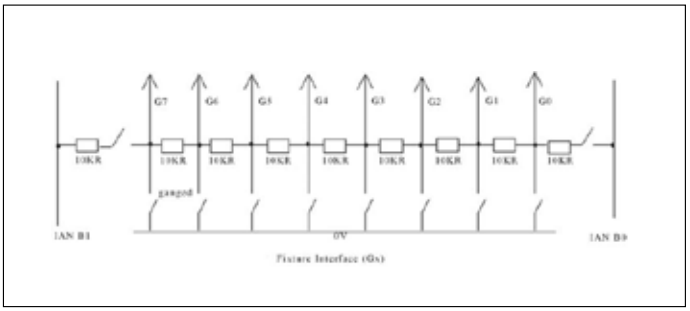
A general-purpose attenuator is included, connected to the internal common bus (IANB) as follows:

Note: The Rmon is a (logic) monitor point for test purposes. (See "Testability Features" for more details.)



Fixture Grounding Pins

Eight pins are routed to ground from the fixture interface via a relay (4 double pole relays altogether). For testing purposes they are wired as follows:



Specification

Analog Routing Path	
Current switching	500 mA DC or AC pk resistive
Current routing	500 mA DC or AC pk resistive
Power switching	10 Watts
Resistance (ANB to fixture interface)	<500 mR
Operating time	300 uS
Release time	150 uS
Isolation	1E11R
Isolation voltage	100 V DC or 100V AC peak
Maximum current	500 mA
Ground Signals	
Current switching	*2 A*
Power switching	*60 W*
Guard Amplifier	
Offset voltage	*+/-1mV*
Bias current	*+/-10 nA*
Amplifier output	*250 mA +/-10 V*
Amplifier inputs+/-10V	*Local feedback*
	100 kR
Input impedance	*10 MR (positive input)*
Attenuator	
TH to TL impedance	*100 kR/0.25 W*
TL to TO impedance	*10 kR/1.0 W*
Withstanding voltage	*100 V*

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