VIAVI Solutions

Data Sheet

VIAVI
Xgig Exerciser
for PCI Express® 5.0

The PCIe Exerciser generates PCIe data streams and responses for compliance testing and analysis

The VIAVI Xgig® PCIe Exerciser brings turn-key compliance test capability to the Xgig PCIe product portfolio. An Exerciser is also a valuable tool for debugging difficult protocol communication problems because it provides full, bit-level, repeatable control over the PCIe data traffic.

An Exerciser generates PCIe complaint data traffic and can respond to PCIe inputs with appropriate branching. It operates in two modes: Root Complex (RC) or host mode and End Point (EP) Mode. In RC emulation mode, the Exerciser enables endpoint testing. In EP mode, the Exerciser enables testing a host system.

The Exerciser supports detailed validation and debug of the state machine of a PCIe controller. It enables debug and performance tuning of firmware and application software. The Exerciser can be programmed to non-compliant PCIe sequences to enable testing of boundary and stress conditions that are not normal to correct system operation and would otherwise be very difficult to evaluate.

The Exerciser works in tight association with the Analyzer function to provide detailed trace capture and full detail of operation. Bidirectional data of hundreds of gigabytes can be saved for detailed analysis using VIAVI tools such as Expert™.

A scripting API is available so that complex, custom Exerciser test scripts can be created; either as original or modified from pre-defined library scripts.

Interposers provide a physical link between the Xgig 5P16 PCIe 5.0 platform chassis and the Device-Under-Test (DUT). Different Interposers support testing of endpoint devices or host systems.

Key Features

- Emuates either a Root Complex or an End Point device
- Generates and responds to PCIe complaint data packets
- Operates to 32GTps, and supports all other PCIe data rates of 2.5, 5.0, 8.0 and 16GTps
- Supports links of 1, 2, 4, 8 and 16-lanes
- Set link rates and widths and control transitions other rates
- Tightly aligned operation with the Analyzer for fully detailed bit-level trace captures
- Execute the PCIe compliance test suite
- Perform LTSSM testing: both positive and negative test scenarios
- LTSSM state tracker with history log
- Define custom test configurations, save and load
- Define custom test suites and execution sequence
- Swap DLLP ACK to NAK responses. Modify CRC.
- Define, send, and modify Ordered Sets
- Scripting API allows complex test cases
- Graphical control interface provides easy visual presentation and setup of test procedures
- Xgig tools and the Exerciser user interface operate on a Windows 10 enabled PC
- Runs on the VIAVI 5P16 Analysis Platform chassis, Xgig5P-PCIe5-X16-PF
- Select appropriate Interposers suitable for your application

Xgig Exerciser Interface – Start Page

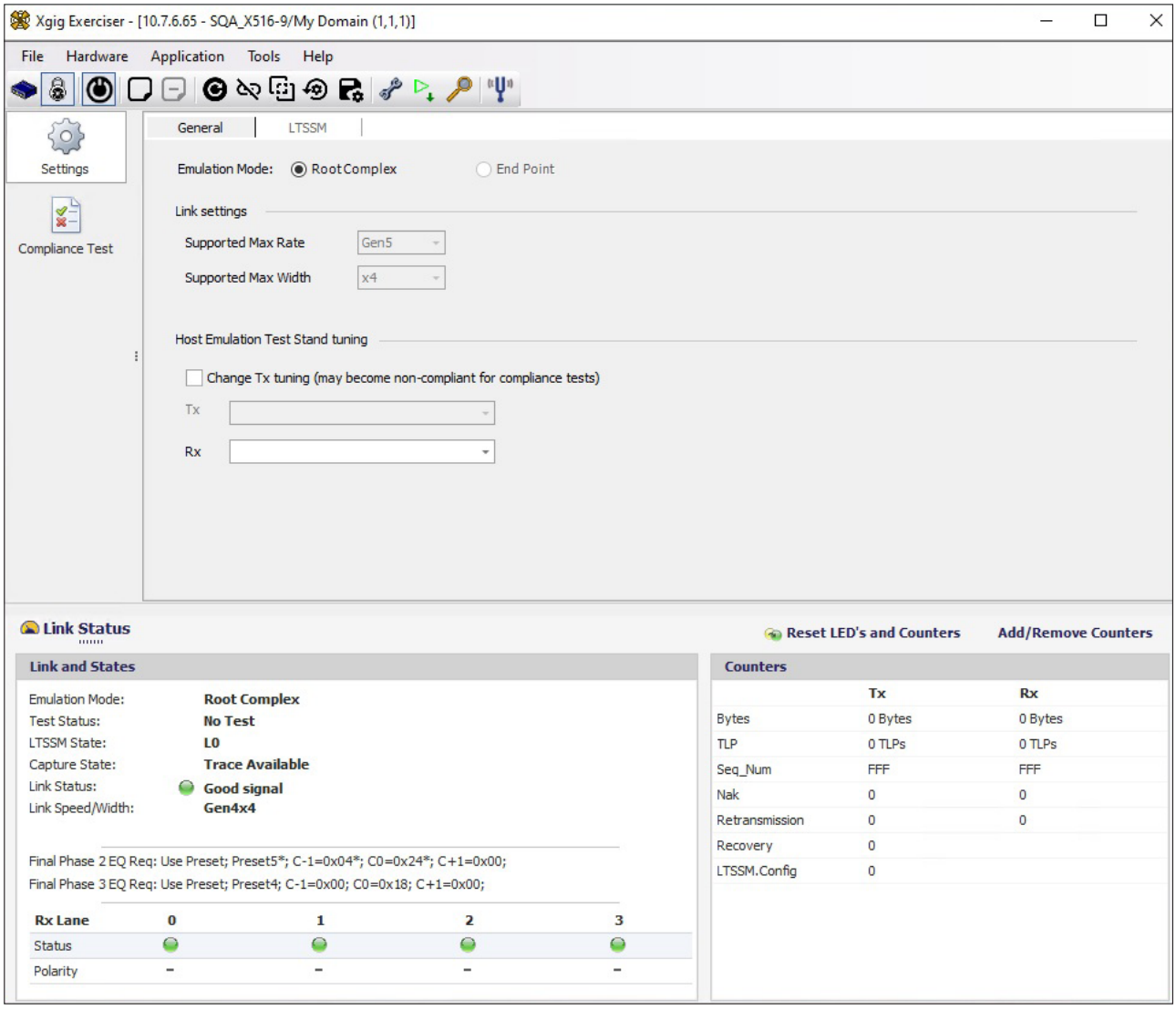

Figure 1 – Exerciser Start Screen

Exerciser User Interface

The Xgig PCIe Exercsier user interface makes it easy to set up and execute a test. Figure 1 above shows the Exerciser launch screen. The top bar includes the typical Windows™ control items. The second bar down has various quick launch buttons for tasks done often.

On the left side are icons for Settings, Compliance Tests, and other features. The Settings>General tab is the first that is presented. Information on the test bench configuration is provided including clocking, reset and other basic controls.

From Settings, controls for the extensive Exerciser parameters are accessible. The LTSSM tab provides control over link settings and operation.

For example, TX and RX setting can be adjusted from this tab. It also allows setting timeouts and other parameters. The Settings tab allows forcing limits on the test data rate and maximum link width.

Below the Settings icon, the Compliance Test icon opens a panel for selecting tests to be run. This is as shown in the next figure.

Below the Compliance Test icon the Config Space icon opens for defining the Exerciser's PCIe configuration space parameters.

Always available at the bottom of the Exerciser window is the current test and bench status.

Xgig Exerciser Interface – Compliance Testing

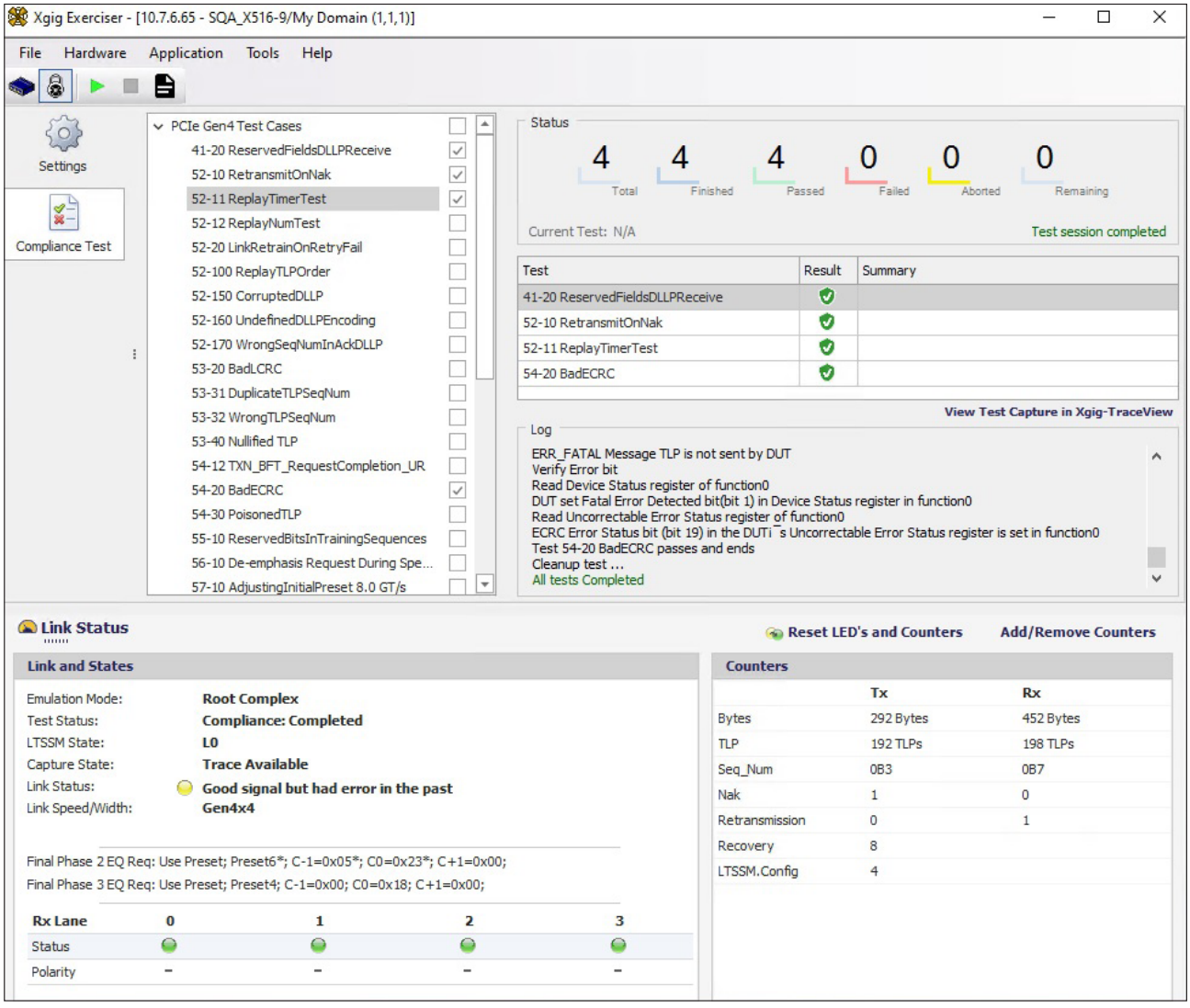

Figure 2. Test Selection Screen

PCIe Compliance Testing

The PCI-SIG performs official certification testing to ensure that every device meets the minimum requirements of the PCIe specification. Testing is done at two levels: (1) Electrical, and (2) Protocol. Electrical testing is performed using BERT and oscilloscope instruments. Protocol testing is performed using PCIe exercisers such as this one.

Compliance testing is an important function of a PCIe Exerciser. The VIAVI Exerciser enables quick pre-certification to the Protocol Compliance test suite. All the PCIe 4.0 tests can be run today.

Tests can be executed individually, in groups, or all in sequence. A simple pass-fail response is provided, and as an option, a full trace of the communication can be saved for detailed analysis if a problem is reported. A detailed trace can help to get problems identified and resolved quickly. An example listing of some of the required Compliance tests is shown in Figure 2 above.

Compliance tests are pre-defined and locked to ensure execution follows PCI specifications. However, they can be copied, edited and saved as a new script to create a similar, but different, test when needed.

Test Applications

The following table lists some of the features available and tests that can be done using the Xgig PCIe Exerciser.

Control and validate reset functions	Define ROM write address space size and offset
Control DUT power	Define Cfg read address space size and offset
LTSSM supported states: Detect, Quiet, Configuration, L0, L1, Recovery	Define Mem64 read address space size and offset
Set data rate	Define Mem32 read address space size and offset
Set link width	Define IO read address space size and offset
Edit LTSSM state transitions	Define ROM read address space size and offset
Control link width changes	Supports Config Space Type 0 Headers (32b)
Control link rate changes	Supports Config Space Type 1 Headers (64b)
Test transitions: any speed/width to any other	Inject disparity errors option
Control link state changes	Inject symbol errors option
Set TX parameters	Inject Sync Bit errors option
Set RX parameters	Define ACK/NACK policies
Control equalization procedure	Control ACK/NACK DLLP generation/reception
Generates TLP 32b memory packets	Auto generate TLP sequence numbers
Generates TLP 64b memory packets	Auto generate TLK LCRC
Generates TLP IO packets	Auto retransmit TLP's that NACK'd
Generates TLP configuration packets	Validate state timeouts
Generates TLP message packets	Set replay timeouts
Execute bad TLP packets	Control SKP generation
Define TS1/TS2 data	Define custom test configurations, save and load
Define Cfg write address space size and offset	Define custom test suites and execution sequence
Define Mem64 write address space size and offset	View test description
Define Mem32 write address space size and offset	View test results
Define IO write address space size and offset	View extensive error count information

Ordering Information

License Keys for up-to 16-lanes, 8-lanes or 4-lanes operation are available to match your specific test needs.

Part Number	Description
Xgig5P-PCIe5-X16-EX	Xgig 16-lane Exerciser License Key for PCIe 5.0
Xgig5P-PCIe5-X8-EX	Xgig 8-lane Exerciser License Key for PCIe 5.0
Xgig5P-PCIe5-X4-EX	Xgig 4-lane Exerciser License Key for PCIe 5.0

VIAVI Solutions

Contact Us **+1 844 GO VIAVI**
(+1 844 468 4284)

To reach the VIAVI office nearest you,
visit viavisolutions.com/contact

xgig-exerciser-ds-snt-nse-ae
30193058 900 0421