

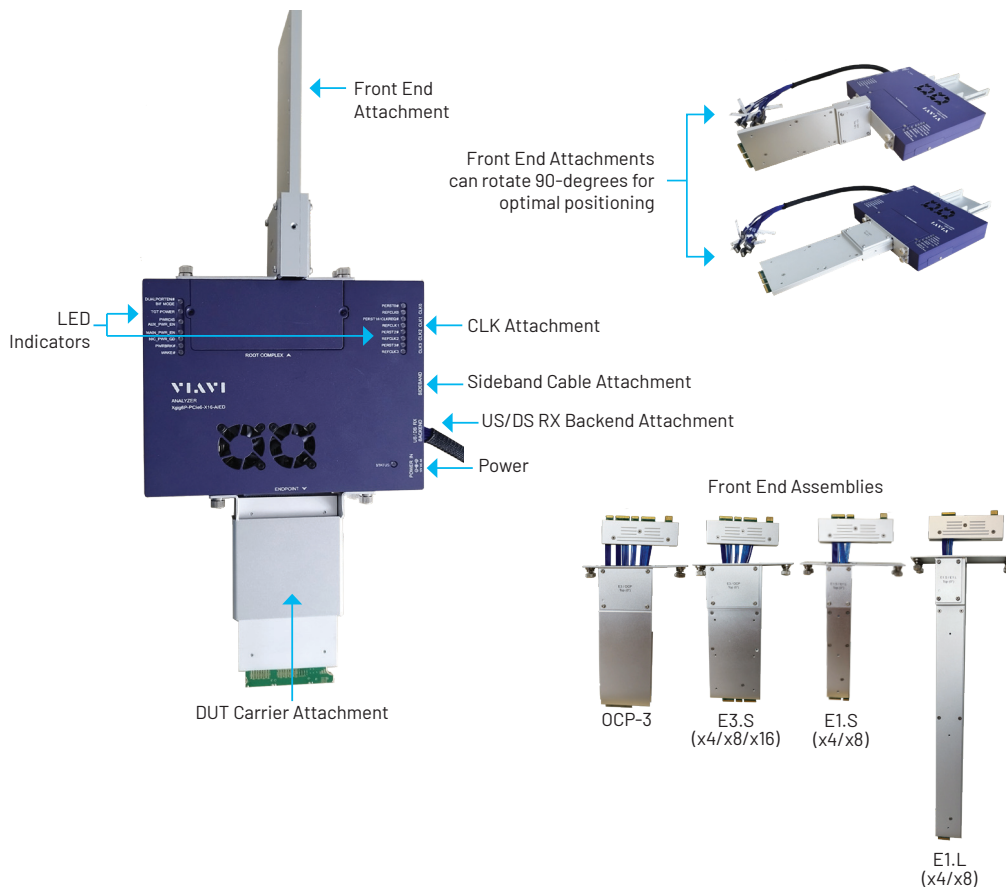
Xgig EDSFF Analyzer Interposers

for PCI Express® 6.0

Provides a high-fidelity tap of data signals between a host system and EDSFF Module for the VIAVI Analyzer

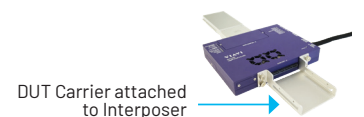
VIAVI Solutions Xgig® EDSFF Analyzer Interposers provide connection between the VIAVI PCIe 6.0 Analyzer/Exerciser Chassis and a system under test for up to 64GT/s x16 capture. The Analyzer Interposer installs into an EDSFF slot to provide a fully analog signal path between the root complex and the endpoint. The Analyzer Interposer provides a tap of the data signal communication between host and endpoint devices for input to the Analyzer/Exerciser chassis. It operates at the 64GT/s, PCIe 6.0 rate, across 16-lanes (bi-directional). Variants are available for x16, x8 and x4 lane widths, with accompanying mechanical support for E1.S, E1.L, E3.S, E3.L, and OCP NIC 3.0 modules.

This Analyzer Interposer uses high-speed linear signal redrivers to buffer system data signals across the Analyzer Interposer between the PCIe slot and PCB fingers. This design ensures a clean signal is delivered to the Analyzer/Exerciser chassis and DUT devices for reliable protocol capture and analysis.



Key Benefits

- Operates at 64GT/s PCIe 6.0 data rates, and supports 2.5, 5.0, 8.0, 16 and 32GT/s PCIe data rates
- A 16-lane EDSFF 4C/4C+ or 2C slot receptacle accepts all EDSFF endpoint DUT modules
- A 16-lane 4C/4C+/2C/1C PCB finger connector installs into host test system's EDSFF slot
- Supplied with high-quality custom data cables to ensure good signal capture with minimal tuning effort
- x16 version supports up to 4 sets of Analyzer side-band signal triggering and capture
- Analyzer Interposer power is independent of host system
- Interposer Dimensions: 210 mm x 165 mm x 35 mm (WxDxH)



Applications

Working together with the VIAVI PCIe 6.0, Analyzer/ Exerciser chassis, this Analyzer Interposer enables debug and verification of new ICs, new system hardware designs, FPGA firmware, validation of system BIOS and software, and supports manufacturing test.

The Xgig EDSFF Analyzer Interposer is inserted into a E1, E3, or OCP-NIC 3.0 slot in the host system, and an EDSFF DUT Carrier is installed into the interposer creating the test data path. Cables connect the Interposer to the VIAVI Protocol Analyzer/Exerciser Chassis.

The diagram to the right indicates the signal path with DUT devices attached. Note that this Analyzer Interposer requires an open DUT system chassis while in use. The Analyzer captures DUT data (tapped) from both the upstream and downstream signal paths as inputs to the Analyzer/Exerciser Chassis.

VIAVI offers a variety of other Interposer types for connecting into many popular PCIe system applications, including CEM, U.2, M.2, CDFP (CopprLink), MCIO (CopprLink), Flying-Lead and others.

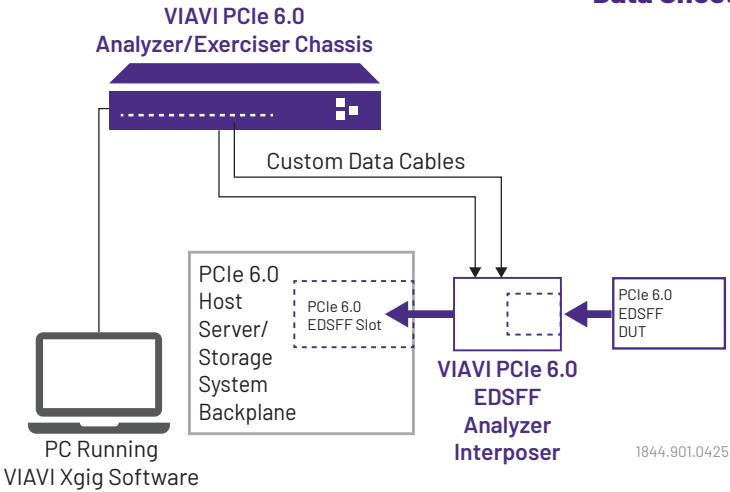


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Kit Contents

Included components will vary by selected products, but typically include cables, cords, brackets and instructions necessary for proper operation of the selected product.

Ordering Information

Part Number	Description
XGIG6P-PCIE6-X16-AIEE	PCIe 6.0 x16 Analyzer Back End EDSFF
XGIG6P-PCIE6-X4-IE1.S	PCIe 6.0 x4 Analyzer/Exerciser Front End EDSFF E1.S
XGIG6P-PCIE6-X8-IE1.S	PCIe 6.0 x8 Analyzer/Exerciser Front End EDSFF E1.S
XGIG6P-PCIE6-AIE1.S	E1.S DUT Carrier
XGIG6P-PCIE6-X4-IE1.L	PCIe 6.0 x4 Analyzer/Exerciser Front End EDSFF E1.L
XGIG6P-PCIE6-X8-IE1.L	PCIe 6.0 x8 Analyzer/Exerciser Front End EDSFF E1.L
XGIG6P-PCIE6-AIE1.L	E1.L DUT Carrier
XGIG6P-PCIE6-X4-IE3	PCIe 6.0 x4 Analyzer/Exerciser Front End EDSFF E3
XGIG6P-PCIE6-X8-IE3	PCIe 6.0 x8 Analyzer/Exerciser Front End EDSFF E3
XGIG6P-PCIE6-X16-IE3	PCIe 6.0 x16 Analyzer/Exerciser Front End EDSFF E3
XGIG6P-PCIE6-AIE3	E3.X DUT Carrier
XGIG6P-PCIE6-x16-IOCP3	PCIe 6.0 x16 Analyzer/Exerciser Front End EDSFF OCP3
XGIG-INTPSR-C-Hx (x=1,2,3,4)	x-year extended hardware warranty