New Perspectives in Test: 400G and the new test revolution

Introduction

Until and through the introduction of 100G, the task of validating and testing client optics was a relatively simple task. An optical module would be operated through a 'test' channel, then the corresponding bit error rate (BER) was measured and used as a pass/fail limit. In most cases, an error-free result was expected over a typical measurement period.

By comparison, 400G client optics have moved from non-return to zero (NRZ) to PAM-4 (pulse amplitude modulation-4) based modulation and now also use forward-error correction (FEC) for all physical medium dependent (PMDs). This advancement significantly complicates optical module test and validation. The relationship between error statistics (and root causes) and the FEC characteristics are intimately linked so a simple pass/fail limit can no longer be used.

This paper describes the new challenges that arise with 400G optics and how they call for a new perspective on test and validation. This new approach will allow a better probability of detecting bad optics and passing good optics without significantly adding to the test burden.

Current 'best practice' with 100G and Lower

At Viavi, we have over thirty years of experience testing and validating client-based optics based on NRZ electrical and optical modulation. Even recent experience testing on 25G- and 40G-based NRZ systems have shown the current links can be treated as 'very low' BER when designed and built properly. The test methodology has been rather simple:

1. Run a simple unframed BER test
2. Count errors (hopefully zero)
3. Accept optics as 'known good' stressors (different patterns, clock rates, skew and even SRS can be added by the ultimate threshold for a pass/fail remains a BER)

This method is ideally suited to client optics that run 'error free' without use of a client FEC (such as the 100G LR4), but is also applicable to other PMDs that nominally require a FEC such as SR4 at 100G. A FEC is required as the physical medium (such as multi-mode fiber) can cause errors on the transmitted data. FEC allows a low-cost physical medium to be used as it can correct many of the errors that occur over the link. The reality is that these optics can run error-free or at very low error rates (below 10^-12) in a 'loopback' so this gives a very simple pass/fail criterion. Indeed, we have a current ecosystem expectation that all client optics should run error-free for at least a 'coffee break' interval in the lab in an optical loopback.

A short introduction to 400G client optics

The IEEE P802.3bs project for 400G (and 200G) is making good progress and standardization is expected around the latter half of 2017. While the Ethernet portion of the draft standard is very familiar, innovative technologies (from a client-side perspective) need to be adopted to allow 400G technology to meet the cost and size expectations of the broader market. Some of these new topics include:

- **PAM-4.** PAM-4 modulation uses 4 levels of signal rather than the 'classic' 0 or 1 used in NRZ. This allows twice as much information to be sent in the same time interval. The gap between the signal levels is much smaller so the signal is more susceptible to noise.
- **FEC.** Forward error correct coding allows a errors in the transmitted signal (which can occur through mechanism including noise, interference and reflections) to be corrected by additional bits of information added during the coding phase. FEC codes have found universal applications in CDs, DVDs, RF and fiber optic communications.
- **Raw error rate.** Raw error rate is the error rate occurring over the physical medium before FEC has corrected any errors.
- **Frame loss.** Frame loss is the number of Ethernet frames lost due to errors that cannot be corrected and so the whole frame of data must be discarded.
- **Mean-time-to-false-frame-acceptance (MTTFFA).** MTTFFA is the mean time a link runs before a data packet is so badly corrupted that the error protection and detection afforded by the FEC code and checksum can no longer indicate a packet is corrupted and so the receiver believes it is actually a 'good' packet or frame.

Why counting bits is no longer relevant

The FEC is not a magic block that can convert all 10^-4 pre-FEC BER into zero-errored-frames post-FEC. In fact, it is heavily impacted by the nature of the error statistics—with the burst length being of particular impact.

It is entirely plausible to have one module which runs at a raw error rate of 10^-4 (and will operate error-free post-FEC as its error distribution is random with bonded burst length) and another module running at 10^-10. However, due to design and performance, the error characteristics of the latter lead to uncorrectable errors. So, a simple BER test—even with a significant guard band (10^6)—can still lead to failing perfectly good modules and passing modules with fundamental performance limitations.

Fingerprint the error statistics

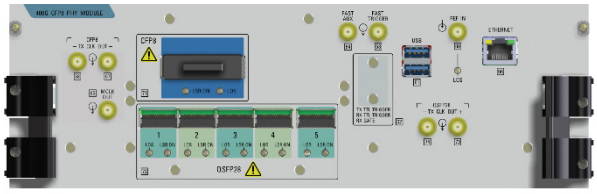
The very nature of the errors requires fingerprinting to determine the error statistics per key parameters such as burst length, burst gap, and whether the burst is a true error or a pattern slip. This level of detail is required to determine the root cause of the errors, to take corrective design action, and to build enough margin into the module to run error-free with the FEC.

With error burst length and nature, there is an upper bond to the length of burst that can be corrected by the FEC. This sets an important limit to the manageable burst length, and with this knowledge you begin to build out an idea of the margin in the module. Questions on the nature of the burst are important: Is it classic bit error, a pattern slip, or a 'flooring'? For example, when errored bits were only "1" or only "0", one would get valuable information on the root cause and therefore allow the appropriate corrective action to be taken. Optimal testing should identify issues with CDR (clock data recovery) bandwidth challenges, pattern sensitivity, and linearity (especially over the demanding dynamic range required at the photonic receiver).

Tools such as bit-capture allow complete visibility of the events leading up to errors and bursts as well as the ability to reconcile the bit capture in terms of the coded PAM-4 signal at the photonic layer. Again, this allows the root cause of errors to be explored and corrected.

A new 'recipe' for module test & validation

With the new 400G test set, you can run a detailed, unframed BER test with a range of aggressive patterns. It's important to target getting the right aggressors in the photonic domain where most of the error budget is allocated. This will require the ability to generate specific PRBS_Q and SSPR_Q patterns via the AUI-8 and AUI-16 interface which correctly translate to the 'true' pattern at the photonic layer.

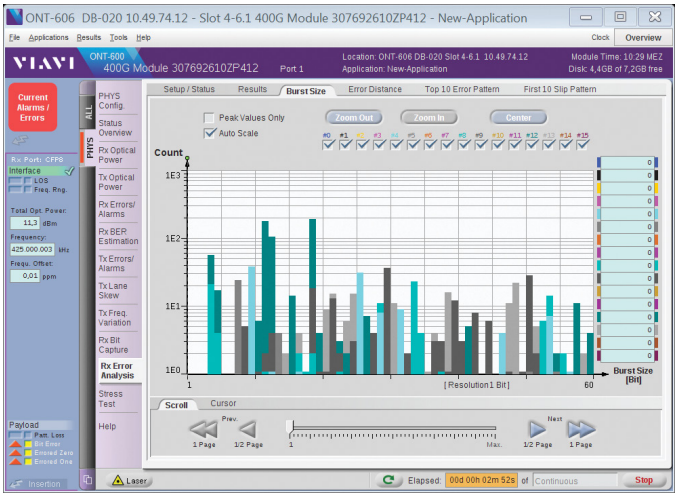


The ONT 400G

You can also use advanced error analysis to fully understand the nature of the errors. The error distribution and statistics are critical—especially with respect to burst errors. The burst length and spacing are crucial parameters for understanding how the FEC will perform. Furthermore, having a detailed understanding of the error statistics means you can, in many cases, address the root cause (CDR performance, bandwidth, electrical or photonic crosstalk, linearity) and drive increased module performance. Of course, it is also important to stress the module during this phase and classic stressors can include:

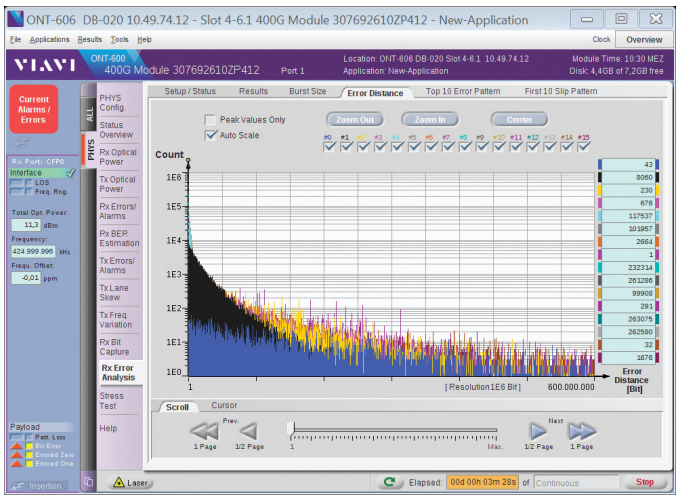
- Aggressive mix of patterns (including SSPR_Q)
- Dynamic skew variation
- Clock rate variation (both ramp and step-change or "jump")
- Jitter injection
- Aggressive control bus activity
  (high duty cycle I^2C or MDIO read/write activity)

These stressors can be used to bring out module design issues and margin. Again, certain failure modes can be investigated to find a root cause and hence drive better module performance.



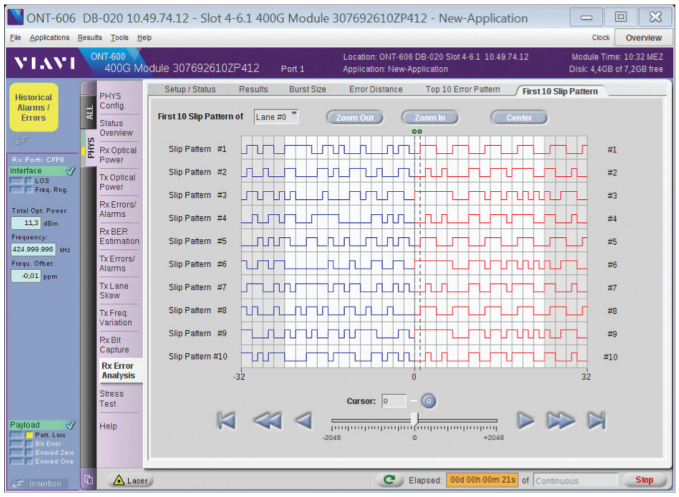
Graphical Tracking of Burst Error Length

An error burst is a case where a number of bits or symbols are corrupted due to a single event. This single event, due to its nature and/or generation, corrupts several bits or symbols within a definitive time window. In this example the burst count versus burst size is shown. It shows a high number of bursts occurring longer than 32 bits, so in this case we may have errors which the FEC cannot correct.



Distance Between Errors

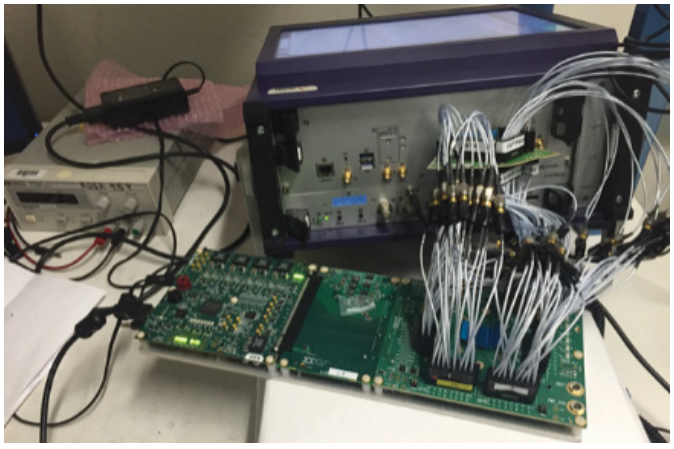
The distance between errors can give valuable insight into the error statistics. In this case, we see a typical roll-off with gap. This is typical of a random Poisson process. Distinct peaks in the error distance indicate some deterministic mechanism which can include a pattern sensitivity, and crosstalk (from power supply unit (PSU) and microcontroller circuitry). For example, a 1 MHz repetition signal burst would couple in at around 25000 bits, such a peak could be clearly recognized with this view.



Capturing and Displaying Pattern Slips

Determining what is an error burst and what is a pattern slip is critical in finding and rectifying the root cause. In this case, the ONT advanced error analysis shows that a pattern slip is occurring. Conventional tools show errors only. By contrast, the developer here has full visibility of the true issue. Bit slips typically occur with the CDR function so this is where investigations should focus.

After the performance of the module has been optimized via unframed deterministic patterns, the module can now be run in a real traffic scenario. Module characteristics are established with live Ethernet traffic and detailed monitoring of pre-FEC and post-FEC error rates (hopefully zero). Of course, this is how the module will be used in the 'real' world, so a live traffic test is a critical step. In this step, the pre-FEC error rate should remain relatively constant and well within the margin the FEC capability. The post-FEC error rate should be zero. With this information and the raw error statistical characters gathered earlier, the module vendor and user will have confidence the module will operate with sufficient margin when deployed in the field.



This photo shows a prototype 400G PAM-4 IC under test using the ONT 400G and its AUI-16 electrical adapter. The novel applications developed by Viavi and deployed on the ONT product family give the insight and knowledge required to fully characterize and test modern optical modules through techniques such as advanced error analysis and framed (with FEC) testing.

A new approach

Through the history of Ethernet technology, the task of validating and testing client optics was relatively simple. Today, as 400G components and modules are developed, a new approach is required to successfully validate and test optics. The complexity of PAM-4 coupled with the highly non-linear behavior of the FEC means we must finally move beyond the simple error counting of the past. The new, more sophisticated approach outlined in this paper enables improved detection of bad optics and passage of good optics without adding a significant burden to the testing phase.

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